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EXAMINER	
LO, SUZANNE	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/731,593	BAECKLER, GREGG	
	Examiner	Art Unit	
	SUZANNE LO	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,20-34,36 and 37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15, 20-34, 36 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15, 20-34, 36-37 have been presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 1-9, 20-28, and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Leaver et al. (U.S. Patent No. 6,195,788 B1) in view of Cong et al. ("Cut Ranking and Pruning: Enabling a General and Efficient FPGA Mapping Solution").**

As per claim 1, Leaver is directed to a method of determining an implementation of a user design on a programmable device including a plurality of programmable logic elements, each comprising reconfigurable logic hardware and fixed-configuration secondary hardware **(column 7, lines 44-51);** the fixed-configuration secondary hardware having a plurality of inputs, the inputs common to at least two of the programmable logic elements **(column 9, lines 28-35)**, the method comprising: for each of a plurality of portions of the user design, *determining one or more sets of input assignments to the fixed-*

configuration secondary hardware, each set providing an implementation of that portion of the user design using the fixed-configuration secondary hardware **(column 9, lines 60-67 and column 9, lines 19-25)**; ranking the *input* assignments **(column 10, lines 1-15, Table 1)**; and selecting the highest ranked *input* assignment as an implementation of at least a subset of the portion of the user design **(column 10, lines 41-64)** but fails to explicitly disclose wherein the ranking the plurality of *input* assignments by determining a number of times each of a plurality of signals in the user design is assigned as *a respective input* to the fixed-configuration secondary hardware, wherein the selecting the highest ranked *input* assignment where a first signal in the plurality of signals in the user design is assigned as a first input to the fixed-configuration secondary hardware more than *any* other *signal* in the user design *is* assigned to an input to the fixed-configuration secondary hardware and implementing the user design by implementing the first signal as the first input to the fixed-configuration secondary hardware.

Cong teaches wherein the ranking the plurality of *input* assignments by determining a number of times each of a plurality of signals in the user design is assigned as *a respective input* to the fixed-configuration secondary hardware **(page 33, Section 3.3.5)**, wherein the selecting the highest ranked *input* assignment where a first signal in the plurality of signals in the user design is assigned as a first input to the fixed-configuration secondary hardware more than *any* other *signal* in the user design *is* assigned to an input to the fixed-configuration secondary hardware **(page 33, Section 3.3.5, 2nd paragraph)** and implementing the user design by implementing the first signal as the first input to the fixed-configuration secondary hardware **(page 33, Section 4)**.

Leaver, and Cong are analogous art because they are from the same field of endeavor, implementing a user design on a programmable device. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of programming a device of Leaver with the steps of ranking and selecting input assignments of Cong in order to provide more freedom in forming different LUTs **(Cong, page 33, Section 3.3.5, 2nd paragraph)**.

As per claim 2, the combination of Leaver and Cong already discloses the method of claim 1, wherein each of the *input* assignments defines an assignment of at least one input variable of the user design to an input of the fixed-configuration secondary hardware **(Leaver, column 7, line 44-51, Figure 4A)**.

As per claim 3, the combination of Leaver and Cong already discloses the method of claim 1, but does not specifically disclose wherein the fixed-configuration secondary hardware enables load and clear functions of a register of the programmable device but it would have been obvious to one of ordinary skill in the art to enable the load and clear functions of the register in order to operate said register.

As per claim 4, the combination of Leaver and Cong already discloses the method of claim 1, wherein each *set* of the *input* assignments is associated with at least one register of the user design **(Leaver, Figure 1C)**.

As per claim 5, the combination of Leaver and Cong already discloses the method of claim 4, wherein ranking the *input* assignments includes determining *a* number of registers of the user design associated with each *input assignment* **(Leaver, Figure 1C)**.

As per claim 6, the combination of Leaver and Cong already discloses the method of claim 5, wherein selecting the highest ranked input assignment includes selecting the *input* assignment with the most associated registers **(Leaver, Figure 1C and Cong, page 33, Section 3.3.5)**.

As per claim 7, the combination of Leaver and Cong already discloses the method of claim 4, comprising disassociating at least one register from at least one of the *input* assignments, wherein the disassociated register is associated with the selected *input* assignment **(Leaver, Figure 1C and Cong, page 33, Section 3.3.5)**.

As per claim 8, the combination of Leaver and Cong already discloses the method of claim 1, comprising removing the selected *input* assignment from the *input* assignments, thereby forming a subset of the *input* assignments **(Cong, page 33, Section 3.3.5)**.

As per claim 9, the combination of Leaver and Cong already discloses the method of claim 8, comprising evaluating a criteria for the subset of the *input* assignments; and in response to a determination that the criteria exceeds a threshold, reiterating the steps of ranking the plurality of assignments and selecting the highest ranked input assignment for the subset of the *input* assignments **(Cong, page 33, Section 3.3.5)**.

As per claims 20-28, the combination of Leaver and Cong is directed to an information storage medium **(Leaver, Figure 7 and column 11, lines 34-60)** including a set of instructions adapted to operate an information processing device to perform a set of steps, the set of steps comprising the method steps of claims 1-2, 4-9, 16-19 and are therefore rejected over the same prior art combination.

As per claim 36, Leaver is directed to a method of implementing a user design on an integrated circuit, the user design comprising a plurality of logic gates and a plurality of registers, the integrated circuit comprising a plurality of programmable logic elements, each programmable logic element comprising a register and a plurality of logic gates having a plurality of inputs **(Figure 1C)**, the method comprising: for each register in the plurality of registers in the user design: determining a logic representation for at least one logic gate having a plurality of inputs **(column 4, lines 28-41)**, the at least one logic gate coupled to the input of the register in the user design **(Figure 1C)**; determining at least one way to implement the logic representation using the plurality of logic gates in a programmable logic element **(column 7, lines 12-25)**; and assigning input signals to the at least one logic gate of the user design to inputs of the logic gates in the programmable logic element **(Figure 4A and column 8, lines 5-25)** but fails to explicitly disclose then for each input signal in a plurality of input signals to the logic gates coupled to input of registers in the user design; determining a number of occurrences where the input signal is assigned to an input of the logic gates in a programmable logic element; and determining a first input signal and first input of the logic gates in the programmable logic elements where the first input signal is assigned to the first input more than other input signals are assigned to an input of the logic gates

in the programmable logic elements; then implementing the user design on the integrated circuit by implementing the first input signal as the first input of the logic gates in the programmable logic elements.

Cong teaches for each input signal in a plurality of input signals to the logic gates coupled to input of registers in the user design; determining a number of occurrences where the input signal is assigned to an input of the logic gates in a programmable logic element **(page 33, Section 3.3.5)**; and determining a first input signal and first input of the logic gates in the programmable logic elements where the first input signal is assigned to the first input more than other input signals are assigned to an input of the logic gates in the programmable logic elements **(page 33, Section 3.3.5, 2nd paragraph)**; then implementing the user design on the integrated circuit by implementing the first input signal as the first input of the logic gates in the programmable logic elements **(page 33, Section 4)**.

Leaver and Cong are analogous art because they are from the same field of endeavor, implementing a user design on a programmable device. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of programming a device of Leaver with the steps of ranking and selecting input assignments of Cong in order to provide more freedom in forming different LUTs **(Cong, page 33, Section 3.3.5, 2nd paragraph)**.

As per claim 37, the combination of Leaver and Cong already discloses the method of claim 36, but does not specifically disclose wherein the logic gates provide load and clear functions for the register in a programmable logic element but it would have been obvious to one of ordinary skill in the art to enable the load and clear functions of the register in order to operate said register.

3. **Claims 10-15 and 29-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Leaver et al. (U.S. Patent No. 6,195,788 B1) in view of Cong et al. ("Cut Ranking and Pruning: Enabling a

General and Efficient FPGA Mapping Solution") **in further view of Wallace (U.S. Patent No. 7,020,855).**

As per claim 10, the combination of Leaver and Cong is directed to the method of claim 2, but fails to specifically disclose wherein determining *one or more sets of input assignments* comprises: enumerating a plurality of sets of input variables associated with the portion of the user design; and creating a plurality of *input* assignments from at least a portion of the sets of input variables. Wallace teaches enumerating sets of input variables **(column 4, lines 44-53)** and creating a plurality of input assignments **(column 4, lines 15-29)**. Leaver, Cong, and Wallace are analogous art because they are both from the same field of endeavor, implementing a user design on a programmable device. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of programming a device of Leaver and Cong with the method of determining input assignments of Wallace in order to offer greater opportunities for optimization **(Wallace, column 4, lines 20-35)**.

As per claim 11, the combination of Leaver, Cong, and Wallace already discloses the method of claim 10, further comprising: creating a logic diagram describing the function of each of the plurality of sets of input variables; and determining from the logic diagram whether the function of each of the plurality of sets of input variables corresponds with at least one function of the fixed-configuration *secondary* hardware **(Wallace, column 4, lines 44-53)**.

As per claim 12, the combination of Leaver, Cong, and Wallace already discloses the method of claim 11, wherein the logic diagram is a truth table **(Wallace, column 4, lines 44-53)**.

As per claim 13, the combination of Leaver, Cong, and Wallace already discloses the method of claim 11, but does not specifically disclose wherein the logic diagram is a Karnaugh map but it would have been obvious to one of ordinary skill in the art to include the above limitation to easily derive complex sets of input variables.

As per claim 14, the combination of Leaver, Cong and Wallace already discloses the method of claim 11, wherein creating a plurality of assignments comprises applying at least one heuristic to each of the plurality of sets of input variables having a function corresponding with at least one function of the fixed-configuration secondary hardware, thereby determining at least one corresponding assignment **(Cong, page 30, Section 3)**.

As per claim 15, the combination of Leaver, Cong and Wallace already discloses the method of claim 10, wherein enumerating a plurality of sets of input variables includes using cut enumeration **(Cong, page 29, Section 1, 2nd paragraph)**.

As per claims 29-34, the combination of Leaver, Cong, and Wallace is directed to an information storage medium **(Leaver, Figure 7 and column 11, lines 34-60)** including a set of instructions adapted to operate an information processing device to perform a set of steps, the set of steps comprising the method steps of claims 10-13 and are therefore rejected over the same prior art combination.

Response to Arguments

4. Applicant's arguments filed 01/08/08 have been fully considered but they are not persuasive.

5. In response to the Applicant's argument that the anchors of Leaver do not disclose particular pieces of hardware in the programmable logic device, the Applicant is directed to column 7, lines 48-51 wherein anchors are registers and I/O ports for hardware pieces.

6. In response to the Applicant's argument that Leaver does not mention determining input assignments to the anchors, the Applicant is directed to column 9, lines 19-25 as anchors are I/O ports with the connectivity diagram (column 7, lines 55-60).

7. In response to Applicant's argument that Leaver does not teach or suggest ranking the input assignments, in the ranking of particular logic cones, with corresponding anchors, the anchors which are I/O port assignments are ranked (column 7, lines 55-60).

8. In response to Applicant's argument that Cong does not teach or suggest ranking the input assignments by determining a number of times each of a plurality of signals in the user design is assigned as a respective input to the fixed-configuration secondary hardware, the Applicant is directed towards page 33 with decomposition wherein the number of nodes are increased and the logic cones with greater number of nodes are ranked higher. As Leaver teaches nodes of a logic cone consisting of LUTs and registers, the increased number of nodes comprises an increased number of registers, the combination of Leaver and Cong teaches the claimed method of ranking input assignments, particularly as embodied in the specification, paragraph [0041] wherein the groups are ranked by the greater number of registers in the groups.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. The prior art made of record is not relied upon because it is cumulative to the applied rejection. These references include:

1. U.S. Patent No. 5,748,488 issued to Gregory et al. on 05/05/98.

2. U.S. Patent No. 6,086,626 issued to Jain et al. on 07/11/00.

3. U.S. Patent No. 6,026,230 issued to Lin et al. on 02/15/00.

4. U.S. Patent No. 7,020,864 B1 issued to Loong on 03/28/06.

5. U.S. Patent No. 6,990,650 B2 issued to Teig et al. on 01/24/06.

6. "BDD-Based Logic Synthesis for LUT-Based FPGAs" published by Vemuri et al. in 10/2002.

7. "Performance evaluation and optimal design for FPGA-based digit-serial DSP functions" published by Lee et al. on 11/15/02.

6. All Claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kamini S Shah/

Supervisory Patent Examiner, Art Unit 2128

Suzanne Lo
Patent Examiner

Art Unit 2128

/SL/
05/23/08